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Search Results -

Term	Documents
(7 AND 20).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	1
(L20 AND L7).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	1

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Search History

DATE: Friday, March 03, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L23	L20 and l7	1	L23
L22	L20 and l6	4	L22
L21	L20 and l5	9	L21
L20	l4 and (indices or index$5 or number$4)	30	L20
L19	l3 and (indices or index$5 or number$4) and l7	5	L19
L18	l3 and (indices or index$5 or number$4) and l6	17	L18
L17	l3 and (indices or index$5 or number$4) and l5	57	L17
L16	l3 and (indices or index$5 or number$4)	1191	L16
L15	l3 and index$5	806	L15
L14	l4 and l7	1	L14
L13	l4 and l6	4	L13
L12	l4 and l5	9	L12
L11	L8 and l7	5	L11

L10	L8 and l6	17	L10
L9	L8 and l5	52	L9
L8	l3 and load and store	657	L8
DB=PGPB,USPT; PLUR=YES; OP=OR			
L7	(712/217)[CCLS]	520	L7
L6	(712/216-219)[CCLS]	1427	L6
L5	(712/2-300)![CCLS]	11905	L5
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3 and scoreboard$3	30	L4
L3	L2 and (exclusive$4 or unique$6) near6 (id$1 or identif$7)	1195	L3
L2	(table or scoreboard$3) near25 entr$4 near25 (valid$7 or invalid$7)	3364	L2
L1	scoreboard$3 near15 entr$4 near25 (valid$7 or invalid$7)	32	L1

END OF SEARCH HISTORY

Issue logic for a 600-MHz out-of-order execution microprocessor

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Abstract
The logic and circuits are presented for a 20-**entry** instruction queue which **scoreboards** 80 registers and issues four ii a 600-MHz microprocessor. The request logic and arbiter circuits that control integer execution are described in additio compaction scheme that maintains temporal order in the queue. The issue logic data path is implemented in 141000 tr 10 mm^2 in a 0.35-μm CMOS process

Index Terms
Inspec

Controlled Indexing
CMOS digital integrated circuits microprocessor chips

Non-controlled Indexing
0.35 micron 600 MHz CMOS process arbiter circuits compaction scheme instruction queue integer ex issue logic logic data path out-of-order execution microprocessor request logic temporal order

Author Keywords
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References

1 B. Gieseke, et al., "A 600 MHz superscalar RISC microprocessor with out-of-order execution," *ISSCC Dig. Tech. P* Feb. 1997.
Abstract | Full Text: PDF (728KB)

2 N. B. Gaddis, J. R. Butler, A. Kumar, and W. J. Queen, "A 56-entry instruction reorder buffer," *ISSCC Dig. Tech. P* Feb. 1996.
Abstract | Full Text: PDF (1068KB)

3 T. Fischer and D. Leibholz, "Design tradeoffs in stall control circuits for 600 MHz instruction queues," *ISSCC Dig. T* 1998.
Abstract | Full Text: PDF (1280KB)

Citing Documents

1 Inherently lower-power high-performance superscalar architectures , Zyuban, V.V.; Kogge, P.M.
Computers, IEEE Transactions on
On page(s): 268-285, Volume: 50, Issue: 3, Mar 2001
Abstract | Full Text: PDF (1616)